10/726,326

1. (Currently Amended) An integrated circuit structure comprising:

first-type transistors and second-type transistors formed on a same substrate,

wherein said first-type transistors and said second-type transistors each comprise:

a gate ~~conductors~~ conductor over channel regions in said substrate;

sidewall spacers adjacent said gate ~~conductors~~ conductor;

source and drain extensions on opposite sides of said channel regions, wherein said sidewall spacers are larger in said first-type transistors than in said second-type transistors; and

silicide regions between portions of said sidewall spacers and said substrate, wherein said silicide regions are larger in said first-type transistors than in said second-type transistors.

2. (Original) The integrated circuit structure in claim 1, wherein said source and drain extensions are spaced further from said channel regions in said first-type transistors than in said second-type transistors.

3. (Canceled).

4. (Original) The integrated circuit structure in claim 1, wherein said sidewall spacers include oxide liners, and

wherein said oxide liners are thicker in said first-type transistors than in said second-type transistors.

5. (Original) The integrated circuit structure in claim 1, wherein said sidewall spacers comprise multiple-layer sidewall spacers, and

wherein said sidewall spacers in said first-type transistors have more sidewall spacer layers than in said second-type transistors.

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6. (Original) The integrated circuit structure in claim 1, wherein said first-type transistors have different performance characteristics than said second-type transistors.

7. (Original) The integrated circuit structure in claim 1, wherein source and drain extensions in said first-type transistors are made of a different material than in said second-type transistors.

8. (Currently Amended) An integrated circuit structure comprising:

P-type field effect transistors (PFETs) and N-type field effect transistors (NFETs) transistors formed on a same substrate,

wherein said PFETs and said NFETs each comprise:

a gate ~~conductors~~ conductor over channel regions in said substrate;

sidewall spacers adjacent said gate ~~conductors~~ conductor;

source and drain extensions on opposite sides of said channel regions, wherein said sidewall spacers are larger in said PFETs than in said NFETs; and

silicide regions between portions of said sidewall spacers and said substrate, wherein said silicide regions are larger in said PFETs than in said NFETs.

9. (Original) The integrated circuit structure in claim 8, wherein said source and drain extensions are spaced further from said channel regions in said PFETs than in said NFETs.

10. (Canceled).

11. (Original) The integrated circuit structure in claim 8, wherein said sidewall spacers include oxide liners, and

wherein said oxide liners are thicker in said PFETs than in said NFETs.

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12. (Original) The integrated circuit structure in claim 8, wherein said sidewall spacers comprise multiple-layer sidewall spacers, and

wherein said sidewall spacers in said PFETs have more sidewall spacer layers than in said NFETs.

13. (Original) The integrated circuit structure in claim 8, wherein said PFETs have different performance characteristics than said NFETs.

14. (Original) The integrated circuit structure in claim 8, wherein source and drain extensions in said PFETs are made of a different material than in said NFETs.

15-28 (Canceled).

29. (Currently Amended) An integrated circuit structure comprising:

first-type transistors and second-type transistors formed on a same substrate,

wherein said first-type transistors and said second-type transistors each comprise:

a gate ~~conductors~~ conductor over channel regions in said substrate;

sidewall spacers adjacent said gate ~~conductors~~ conductor;

source and drain extensions on opposite sides of said channel regions, and

silicide regions between portions of said sidewall spacers and said substrate,

wherein said silicide regions are larger in said first-type transistors than in said second-type transistors,

wherein said sidewall spacers include oxide liners, and

wherein a difference in size of said silicide regions between said first-type transistors and said second-type transistors corresponds to ~~modulated by~~ a difference in thickness of said oxide liners between said first-type transistors and said second-type transistors.

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30. (Previously Presented) The integrated circuit structure in claim 29, wherein said source and drain extensions are spaced further from said channel regions in said first-type transistors than in said second-type transistors.

31. (Previously Presented) The integrated circuit structure in claim 29, wherein said sidewall spacers comprise multiple-layer sidewall spacers, and

wherein said sidewall spacers in said first-type transistors have more sidewall spacer layers than in said second-type transistors.

32. (Previously Presented) The integrated circuit structure in claim 29, wherein said first-type transistors have different performance characteristics than said second-type transistors.

33. (Previously Presented) The integrated circuit structure in claim 29, wherein source and drain extensions in said first-type transistors are made of a different material than in said second-type transistors.

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